MPC5553DEMO

Development Board for the Freescale MPC5553

OPTIONS and CONNECTIONS

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Cautionary Notes

1) Electrostatic Discharge (ESD) prevention measures should be applied whenever handling this product. ESD damage is not a warranty repair item.

2) Axiom Manufacturing reserves the right to make changes without further notice to any products to improve reliability, function or design. Axiom Manufacturing does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under patent rights or the rights of others.

3) EMC Information on the MPC5553DEMO board:

a) This product as shipped from the factory with associated power supplies and cables, has been tested and meets with requirements of CE and the FCC as a **CLASS A** product.

b) This product is designed and intended for use as a development platform for hardware or software in an educational or professional laboratory.

c) In a domestic environment this product may cause radio interference in which case the user may be required to take adequate prevention measures.

d) Attaching additional wiring to this product or modifying the products operation from the factory default as shipped may effect its performance and also cause interference with other apparatus in the immediate vicinity. If such interference is detected, suitable mitigating measures should be taken.

Terminology

This development board applies option selection jumpers. Terminology for application of the option jumpers is as follows:

Jumper on, in, or installed = jumper is a plastic shunt that fits across 2 pins and the shunt is installed so that the 2 pins are connected with the shunt.

Jumper off, out, or idle = jumper or shunt is installed so that only 1 pin holds the shunt, no 2 pins are connected, or jumper is removed. It is recommended that the jumpers be idled by installing on 1 pin so they will not be lost.

This development board applies hardwired option selections (VRL_EN and CUTAWAY 1 – 16). These option selections apply a circuit trace between the option pads to complete a default connection. This type connection places an equivalent Jumper Installed type option. The circuit trace between the option pads maybe cut with a razor blade or similar type knife to isolate the default connection provided. Applying the default connection again can be performed by installing the option post pins and shunt jumper, or by applying a wire between the option pads.

MPC5553DEMO Configuration

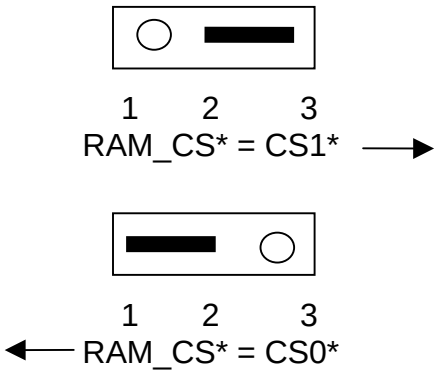
CONFIG Switch

The CONFIG switch provides reset configuration options for the MPC5553 device. Configuration options are enabled by position 1 of the switch. Switch positions 2 – 6 OFF provide an active low output condition to the respective configuration signal. Switch position ON will provide an active high signal condition.

POSITION	CONFIGURATION SIGNAL	DESCRIPTION
6	WKPCFG	**ON = default**, Refer to Freescale MPC5553 Documentation
5	PLLCFG1	**OFF = default**, Refer to Freescale MPC5553 Documentation
4	PLLCFG0	**ON = default**, Refer to Freescale MPC5553 Documentation
3	BOOTCFG1	**OFF = default**, Refer to Freescale MPC5553 Documentation
2	BOOTCFG0	**ON = default**, Refer to Freescale MPC5553 Documentation
1	CONFIG enable	**OFF= default.** ON = enables the RCON configuration to be applied from the switch settings.

SRAM_SEL Option

The MPC5553DEMO board provides a 256K x 18 synchronous SRAM (U2) on the 16 bit data bus D0 – D15. SRAM data bits 16 and 17 are not applied. SRAM_SEL provides selection of the CS0 or CS1 chip selects to access the external SRAM (U2) on the DEMO board. Chip select configuration should be set for 0 wait states, 512K byte memory range, WE signals = Write Enable. The SRAM supports 4 word BURST mode access also.



POWER Supply

This section covers the MPC5553DEMO board power supplies and options. The primary power supply is the MC33394 Power Oak device configured to support the MPC5553 device. The MPC5553 VRC regulator provides the VDD (1.5V) supply in the default configuration (CT1 and CT4 Open, CT2 and CT3 closed). Power Oak 1.5V supply may be applied by optional configuration to provide the VDD 1.5V supply (CT1 and CT4 closed, CT2 and CT3 open).

Power On Reset is provided to the MPC5553 by the Power Oak PORESETB output by default (S0 option closed). The Power Oak HRESETB signal may be applied instead by S1 closed and S0 open.

Power Oak controls are provided by MPC5553 QSPIA. These signals maybe isolated for other applications by opening options S2 – S5.

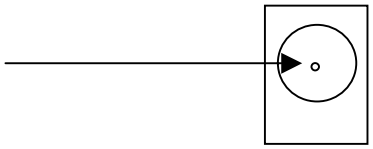
ON_OFF Switch

The ON_OFF toggle switch provides ignition on and off control to the MC33394 Power Oak supply. The Power Oak device will enable and disable the main power supplies. With the switch in the ON position, all power indicators should light. Inspect input power connection and source, and fuse F1 if power indication does not occur.

PWR - Power Jack

The Power Jack provides the default power input to the board. The jack accepts a standard 2.0 ~ 2.1mm center barrel plug connector (positive voltage center) to provide the +VIN supply of +6 to +24 VDC (+12VDC typical).

+Volts, 2mm center



POWER Port

Power Port provides access to the main power supplies and Power Oak optional supplies. The +V connections provided at pins 1 and 2 should be applied for an output voltage source only, not for input supply.

PIN #		SIGNAL DESCRIPTION
1	2	+V = DC input voltage from PWR jack with fuse and polarity protection.
3	4	+5V = regulated +5V supply from Power Oak
5	6	+3.3V = regulated +3.3V supply from Power Oak
7	8	+1.5V = regulated +1.5V supply from Power Oak
9		VDD = MPC5553 VDD supply, 1.5V typically
	10	Ground / VSS
11		VSTBY = MPC5553 VSTBY supply, See VSTBY switch option.
	12	RESET* = MPC5553 Reset input signal.
13		+5VA = MPC5553 Analog supply
15		VREF1 = Power Oak optional +5V output supply, see MC33394 user guide.
17		VREF2 = Power Oak optional +5V output supply, see MC33394 user guide.
19		VREF3 = Power Oak optional +5V output supply, see MC33394 user guide.
21		VSEN = Power Oak switched +V supply output, see MC33394 user guide
23		VPRE = Power Oak mains supply prior to regulation, tap, test, or monitor point.
	24	Ground / VSS
25	26	Ground / VSS

Note: Pins 14, 16, 18, 20, and 22 not connected.

FUSE – F1

Input power is limited by fuse F1. An 5x20mm type 1A slow-blow type fuse is applied to protect the DEMO board for overload conditions.

VSTBY Switch, RV3, and CT7

The VSTBY SWITCH provides enabling and disabling the VSTBY operation of the MPC5553 internal RAM. Switch in the OFF position disables the VSTBY operation and the VSTBY pin is connected to VSS / Ground. Switch in the ON position applies the VKAM standby voltage from the Power Oak supply to the VSTBY pin.

Potentiometer RV3 provides adjustment of the VSTBY voltage from .75 to 1.25 volts. The factory setting for RV3 is VSTBY = 1.0 volts and switch is ON.

Cut-away option CT7 allows the user to isolate the VSTBY pin of the MPC5553 from the switch. With CT7 open, the user must apply external battery or ground to the VSTBY position on the Power Port connector or I/O header ring.

ANALOG Supplies

The MPC5553 +5VA analog supply is provided by the Power Oak VPP regulator output. Individual noise filters are applied to the +5VA supply to derive the VDDA1 and VDDA2 supplies to the MPC5553. VRH reference supply is provided by +5VA default with the VRH_EN option jumper installed. External VRH reference may be applied by removing the VRH_EN option jumper and applying reference voltage at header ring I/O pin A9 or pin 1 of the option header.

The analog ground supply is also noise filtered and provided to the MPC5553 VSSA pins. VRL is provided by option VRL_EN which is a cut-away type option.

The QADC digital supply is provided +5V by option CT9. An optional connection to +3.3V for the QADC is provided by CT10. CT9 must be opened to install CT10 for +3.3V operation. See the MPC5553 user manual for more details on operating the QADC at +3.#V and limitations of the VDDA and VRH supplies. The Power Oak may be set via the SPI control port to provide a +3.3V analog supply on the VPP output. Refer to the MC33394 user manual for details.

USER Components

The DEMO board provides an External clock option (X1), 8 LED indicators, an 8 position DIP switch, 4 push switches, a speaker with amplifier, and 2 user potentiometers. These devices are accessed via the USER LED, USER SWITCH, and USER DEV I/O headers. DEMO board user may apply the devices to the MPC5553 I/O header signals to evaluate operation or assist in code development.

X1 CLOCK Oscillator

The X1 socket is provided to install standard 5V compatible CAN type clock oscillators so that alternate clock source or frequencies maybe applied to the MPC5553. User should refer to the MPC5553 device user manual for information on frequency selection and clocking configuration.

X1 clock signal is provided to the MPC5553 by option pad set CT16 being closed by 0 ohm resistor or mod wire application. CUT-AWAY option CT5 must be opened to remove the Y1 crystal from the EXTAL signal or problems may occur with operation. User should review the MPC5553 user guide for proper PLLCFG0 and PLLCFG1 (CONFIG Switch 4 and 5) option settings if an external clock is applied.

RV1 and RV2 User Potentiometers

The User Potentiometers provide an adjustable linear voltage output from 0 to 5V. The voltage signal may be applied to an MPC5553 analog input port for user application.

USER LED

User LED header provides access to the user LED 1 to 8. Connector pin 1 to 8 organization is provided in a one to one method to the individual indicators LED 1 to 8. The LED indicators are buffered for minimal drive current requirement (~300ua). Indicators will turn on with a logic high or 2.5 to 5V input at the respective connector pin.

USER Switch

User Switch provides access to the user 8 position DIP Switch. Connector pin 1 to 8 organization is provided in a one to one organization to the individual DIP switch positions 1 to 8. The switch connections are pulled low with 10K ohm resistors when the switch position in the off position. Switch positions placed in the ON position will provide a 3.3V output to the connector.

USER_DEV

User DEV provides access to the 4 push switches (SW1 – SW4), speaker, and 2 user potentiometers (RV1 and RV2).

PIN #	USER COMPONENT CONNECTION
1	SW1 out, de-bounced CMOS drive 0 or 3.3V, active low.
2	SW1 out, de-bounced Open Drain output, active low, 10K ohm pull-up to 3.3V. Suitable for IRQ input signal drive.
3	SW2 out, active low, 10K ohm pull-up to 3.3V.
4	SW3 out, active low, 10K ohm pull-up to 3.3V.
5	SW4 out, active low, 10K ohm pull-up to 3.3V.
6	SPEAKER amp input. 0 to 5Vpp, volume adjust with SPKR_VOL.
7	RV1 center tap, 0 – 5V adjustment
8	RV2 center tap, 0 – 5V adjustment

SW1 – SW4 Push Switches

The push switches provide momentary active low input for user applications. SW1 has additional features of being de-bounced for no glitch operation and push-pull output on pin 1 or open drain output on pin 2. Typical user application would be to provide program control or menu selection input.

SW3_UP and SW4_Down are also provided for the UNI_3 Port motor control operation when the MOTOR_EN option is installed.

SPEAKER and SPKR_VOL

The speaker and amplifier provide user applications with a method to generate sound effects from a MPC5553 output. Frequency range of the amplifier input is 300Hz to 10Khz. The SPKR_VOL potentiometer allows user adjustment of the sound effect volume from the speaker. The amplifier also provides a SHDN input connection pad. This pad maybe connected to a MPC5553 output signal to disable the amplifier with a logic high signal of 3.3V or 5V.

MPC5553DEMO I/O Ports

J1 - 10/100TX Ethernet Port

MPC5553 signals D16 – D31 are applied as the FEC module I/O port for Ethernet 10/100TX support provided at J1. FEC signals are applied to U11 (DP83848) 10/100TX PHY device. The J1 port provides AUTO MDIX cable connection detection for standard cross over or straight through type Ethernet CAT5E cables. Three Ethernet status indicators are provided for Link, Speed, and Activity. The PHY device may also be included in the JTAG scan signals by option JP8. Default configuration is PHY not included the scan.

LNK, SPD, and ACT Indicators

Ethernet status is provided by the LNK (Link status), SPD (10 or 100 speed status), and ACT (transmit status) indicators. All three indicators present Green for the active condition as follows:

LNK = ON for Ethernet network link detected. No link detected if off.
SPD = ON for 100TX operation. 10TX operation if off.
ACT = ON for MPC5553 transmit activity. Off indicates idle.

The status indicator operation can be modified by MAC PHY commands. Refer to the DP83848 and MPC5553 user manual for operation details.

JP8 JTAG Scan Option

JP8 is hardwired to exclude the U11 PHY device from the JTAG scan from the JTAG Port. To include the device in the JATG scan, the user should cut the hardwired trace between JP8 pins 2 and 3, install a .1 space 3 pin header, and a jumper shunt option. With the jumper installed on JP8 pins 1 and 2, the PHY will be included in the JTAG scan as the 2nd device.

NOTE: JP8 function is disabled on the Revision B DEMO board, do not apply.

J1 Connector

J1 provides the RJ45 style Ethernet 10/100TX port connection. The connector has an integrated transformer for network connection.

J1 connection

Pin #	Signal
1	TX+
2	TX-
3	RX+
4	TX termination
5	TX Termination
6	RX-
7	RX Termination
8	RX Termination

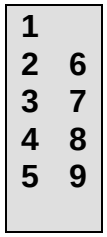
COM-1 Port

COM-1 is a standard RS232 type serial port configured for direct connection to a PC COM Port with a straight through type 9 pin serial cable. Option JP2 provides MPC5553 SCI channel 'A' signal connections when installed. Optional RTS and CTS hardware flow control connection pads are provided for the user to apply MPC5553 I/O ports and software to enhance operation.

JP2 Option

The JP2 Option provides MPC5553 RXDA and TXDA signals to the COM1 transceiver connections. This allows the user to apply the provided communication transceiver with the SCI A channel or to apply the associated I/O to other purposes. JP2 position 1 installed enables the TXDA output and position 2 enables the RXDA input on COM-1.

COM1



The **COM-1** port is a Female (socket type) DB9 connector.

Pins 1, 4, and 6 connected for status null to host.

Pins 7 and 8 maybe applied by CTS and RTS pads to MPC5553 I/O.

RTS signal active output level is logic 0. User should place I/O port applied at logic low (0) to enable the RTS signal and reception of bytes if applied. User should apply a logic high signal under software control inform host or connected RS232 device to STOP transmitting (stop sending incoming bytes).

CTS signal active input is level is logic 0. User should apply software to detect a logic high signal or rising edge on applied I/O port and STOP transmitting bytes to the host or connected device to implement hardware flow control. Detection of a logic low input indicates the host is ready to receive bytes and the user may transmit.

DB9 connector pin locations are provided access pads behind the connector on the DEMO board. User may isolate the connection pads by cutting the associated circuit trace on the bottom of the board.

CAN Port

The CAN Port provides 9 pin connector with the Power Oak CAN transceiver interface to the MPC5553 CAN channels. The CAN_SEL option locations select the CAN channel is applied to the transceiver and CAN Port. User may apply more than one MPC5553 CAN channel to the port if open drain TX output type is applied on the associated CAN channel transmit pins.

CAN_SEL Option

The CAN_SEL option header allows selection of the MPC5553 CAN channels applied to the Power Oak transceiver and CAN Port. If more that one transmit channel is applied, transmit pins must apply the open drain output feature.

Note that the MPC5553 only provides CAN channels A and C, channel B support is provided for MPC5554.

POSITION #	MPC5553 CAN SIGNAL
1	CNTX_A, channel A TX out (**DEFAULT enabled**)
2	CNRX_A, channel A RX in (**DEFAULT enabled**)
3	CNTX_B, channel B TX out (N/A with MPC5553)
4	CNRX_B, channel B RX in (N/A with MPC5553)
5	CNTX_C, channel C TX out
6	CNRX_C, channel C RX in

Following is the DB9S connection reference.

CAN_PORT

1	**1**		X
CAN_LO	**2**	**6**	GND
GND	**3**	**7**	CAN_HI
4	**4**	**8**	8
5	**5**	**9**	9

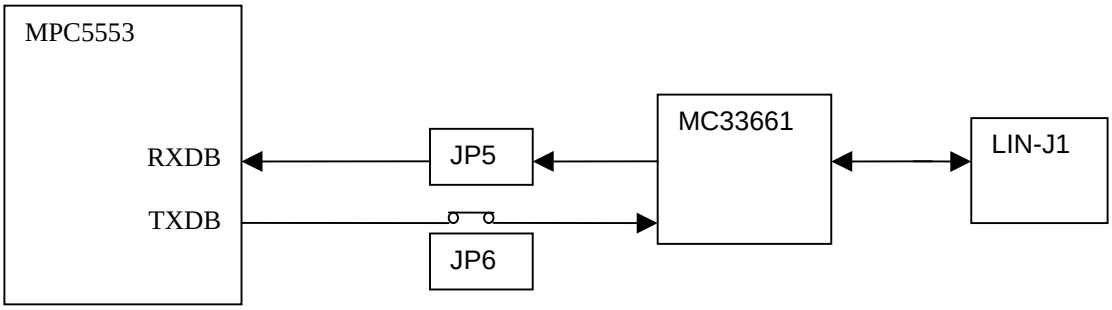
CAN port has a Female (socket type) DB9 connector.

CAN_HI and CAN_LO signals are terminated together with 120 ohms (R68).

DB9 connector pin locations are provided access pads behind the connector on the DEMO board for additional user application.

LIN_J1

The LIN_J1 port provides a Master Mode LIN network connection. The MPC5553 device provides a LIN Master type node on the LIN Network. A LIN physical layer transceiver U7 (MC33661, or similar) is provided between the MPC5553 device and the LIN network connector. Refer to the MC33661 data sheet for complete details of transceiver operation. The following diagram represents the LIN connection:



The LIN interface provides optional features of slew rate control, network supply, and wake up option. See the JP4, JP5, JP6, JP7 and CT8 options following.

CT8 Option

MPC5553 I/O signal GPIO205 provides LIN transceiver U7 enable control (EN pin). Software control of the EN pin allows the user to set the slew rate control of the transceiver. User applications should configure the GPIO205 pin for output to operate the LIN transceiver. If GPIO205 is needed for other purposes, the CT8 option maybe cut to isolate the signal from the LIN transceiver and JP4 installed to provide an enable to the transceiver. Refer to the MC33361 data sheet for further details of operation.

JP4 Option

Installation of JP4 applies a pull-up resistor on the LIN transceiver enable pin. MPC5553 GPIO205 may still control the transceiver enable operation when JP4 is installed.

JP5 Option

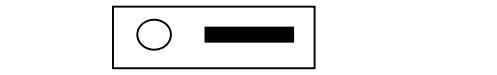
JP5 selects the MPC5553 SCI RXDB signal input to be from the LIN transceiver. For LIN operation JP5 must be installed.

JP6 Option

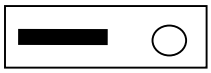
JP6 is wired closed by default and not populated. JP6 provides the MPC5553 TXDB signal to the LIN transceiver. User may cut the JP6 wire trace to isolate the TXDB signal.

JP7 Option

LIN-J1 connector pin 2 may be configured for different network requirements by JP7. JP7 open will disconnect LIN-J1 pin 2 from the DEMO board.



LIN-J1 pin 2 = Ground / VSS ⟶



⟵ LIN-J1 pin 2 = Transceiver WAKE pin

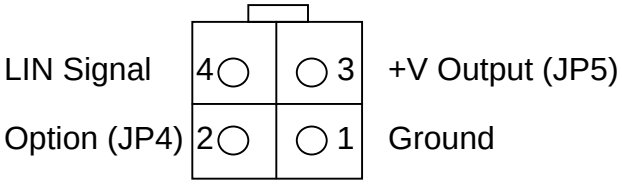
LIN_PWR Option

Installation of the LIN_PWR option applies MPC5553DEMO +V input voltage for LIN network power to LIN-J1 pin 3. This connection allows the DEMO board to operate as a LIN master node to power remote LIN slave nodes. User should use caution to not overload the F1 fuse and verify only one source is applied on the network.

LIN-J1 Connector

The LIN-J1 network connector provides a standard pin configuration with a network option position on pin 2.

Front view (looking into connector from outside of board edge)



Mating connector = Molex 39-01-2040 with 39-00-0039 pins.

UNI_3 Motor Control Port

The UNI_3 Motor Control Port is provided for easy application of the Freescale UNI_3 Motor control application boards and motors. Many of the MPC5553 I/O signals are applied for the UNI_3 motor control application so the user should review I/O application carefully. UNI_3 port operation is enabled by the MOTOR_EN option jumper installation.

MOTOR_EN Option

This option controls the connection of the MPC5553 I/O ports to the UNI_3 and HALL_ENCODER motor control ports. When installed, signal buffers U13 and U15 are enabled to apply MPC5553 I/O for motor control.

UNI_3 Port

The UNI_3 port is the primary motor control I/O port for application of the UNI_3 motor control development boards. Following are the signal assignments:

MPC5553 Signal	UNI_3 Signal	UNI_3 Port		UNI_3 Signal	MPC5553 Signal
TPU_A8	PWM_AT	1	2	Common 4,6,8,10	x
TPU_A9	PWM_AB	3	4	Common 2,6,8,10	x
TPU_A10	PWM_BT	5	6	Common 2,4,8,10	x
TPU_A11	PWM_BB	7	8	Common 2,4,6,10	x
TPU_A12	PWM_CT	9	10	Common 2,4,6,8	x
TPU_A13	PWM_CB	11	12	GROUND	VSS / GROUND
VSS / GROUND	GROUND	13	14	x	
	x	15	16	x	
VSSA	ANALOG GND	17	18	ANALOG GND	VSSA
	x	19	20	x	
AN16	VS_DCB	21	22	IS_DCB	AN17
AN18	IS_A	23	24	ISB	AN19
AN20	IS_C	25	26	x	
	x	27	28	x	
TPU_A15	BRAKE	29	30	x	
	x	31	32	x	
	x	33	34	ZX_A	TPU_A5
TPU_A6	ZX_B	35	36	ZX_C	TPU_A7
	x	37	38	BEMF_A	AN21
AN22	BEMF_B	39	40	BEMF_C	AN23

HALL ENCODER Port

The Hall encoder port is provided for motor position feedback signals from the UNI_3 motor application development boards.

HALL Port	HALL Signal	MPC5553 Signal
1	+5V	+5V / VDDH
2	GROUND	VSS / GROUND
3	H_1	TPU_A1
4	H_2	TPU_A2
5	H_3	TPU_A3
6	H_4	TPU_A4
x	H_CLK	TCRCLK_A, H_CLK is derived by logic from the H_1 – 4 signals.

RUN STOP Switch

The RUN STOP switch is connected to the MPC5553 EMIOS11 signal pin. The switch provides a motor run or stop condition input for the motor control application.

RV4 FAULT Adjust and Fault Indicator

RV4 Fault Adjustment is provided to set the applied motor over-current fault condition. The IS_DCB current sense input from the UNI_3 port is compared by U16 with the RV4 setting to determine if an over-current condition exists. If the IS_DCB input signal is greater than the RV4 setting, the Fault condition becomes active. The FAULT indicator will light and an active low Fault signal will be provided to MPC5553 EMIOS10 signal pin.

SW3_UP and SW4_Down

User switches SW3 and SW4 provide the motor speed UP and DOWN input signals when the MOTOR_EN option is installed. Both switches are active low. SW3_UP signal is provided to the MPC5553 EMIOS8 signal pin. SW4_DOWN signal is provided to the MPC5553 EMIOS9 signal pin.

TPU Port

The TPU_PORT provides an organized I/O port for the MPC5553 TPU_A signals.

MPC5553 Signal	TPU Port		MPC5553 Signal
+3.3V	1	2	+5V
ETPU_A16	3	4	x
ETPU_A17	5	6	x
ETPU_A18	7	8	ETPU_A0
ETPU_A19	9	10	ETPU_A1
ETPU_A20	11	12	ETPU_A2
ETPU_A21	13	14	ETPU_A3
ETPU_A22	15	16	ETPU_A4
ETPU_A23	17	18	ETPU_A5
ETPU_A24	19	20	ETPU_A6
ETPU_A25	21	22	ETPU_A7
ETPU_A26	23	24	ETPU_A8
ETPU_A27	25	26	ETPU_A9
ETPU_A28	27	28	ETPU_A10
ETPU_A29	29	30	ETPU_A11
ETPU_A30	31	32	ETPU_A12
ETPU_A31	33	34	ETPU_A13
GND	35	36	ETPU_A14
TCRCLK_A	37	38	ETPU_A15
GND	39	40	GND

DEVELOPMENT PORTS

The MPC5553DEMO board provides 1 JTAG and 2 NEXUS type development ports. Only one of the development ports should be applied due to common signals used on the ports. The development port input and power signals are buffered by a CBTLV3861 device. This buffer provides a bi-directional 5 ohms series resistance on the input signals when powered on. The buffer also provides signal isolation when powered off.

NOTE: Proper power sequencing must be performed when a development port is applied (cable connected). Development port application power sequence:

1) MPC5553DEMO board ON–OFF switch is OFF and no power is applied to the PWR connector.

2) Connect development port cable to the desired MPC5553DEMO board development port.

3) Apply power to the MPC5553DEMO board PWR connector and turn ON–OFF switch ON.

4) If power is removed or the ON-OFF switch is turned off, remove development cable from board connector and re-apply from step 1 of this procedure.

JTAG Port

The JTAG port provides a Freescale standard JTAG connection to the MPC5553. The connector is a standard 2x7, .1 inch pin space keyed pin header. Example compatible cables include the OCDEMON™ NP-JTAG ONCE “Wiggler” and the P&E Microcomputer Systems CABPPCNEXUS. Host software must be applied to operate the cables.

JTAG Port

Signal	Pin #	Pin #	Signal
B_TDI	1	2	GND
TDO	3	4	GND
B-TCK	5	6	GND
JTG7 TP	7	8	JTG8 TP
B-RESET*	9	10	B_TMS
B_+3.3V	11	12	GND
B_RDY*	13	14	B_JCOMP

Notes:
1) B_… signals are buffered.
2) JTGx TP signals are not connected to the MPC5553 and provide a Test Pad on the board.
3) Signals followed by a “*” symbol are active logic low.
4) See the J1 Ethernet section about JP8 and the PHY device JTAG.

NEXUS Port

The NEXUS port provides a more powerful and higher speed development port for high end tools. The port connector is an AMP 38 pin Mictor style, part number #767053-1.

NEXUS Port

Signal	Pin #	Pin #	Signal
NXS1 TP	1	2	NXS2 TP
NXS3 TP	3	4	NXS4 TP
MDO9	5	6	CLKOUT
BOOTCFG1	7	8	MDO8
B_RESET*	9	10	B_EVTI*
TDO	11	12	B_+3.3V
MDO10	13	14	B_RDY*
B_TCK	15	16	MDO7
B_TMS	17	18	MDO6
B_TDI	19	20	MDO5
B_JCOMP	21	22	MDO4
MDO11	23	24	MDO3
ERSTOUT*	25	26	MDO2
NXS27 TP	27	28	MDO1
NXS29 TP (Note 3)	29	30	MDO0
+V	31	32	EVTO*
+V	33	34	MCKO
NXS35 TP (Note 3)	35	36	MSEO1*
B_VSTBY	37	38	MSEO0*

Notes:
1) B_… signals are buffered.
2) NXSxx TP signals are not connected to the MPC5553 and provide a Test Pad on the board.
3) NXSxx signal TP is also connected to the ROBUST Nexus connector.
4) Signals followed by a “*” symbol are active logic low.

ROBUST Port

The ROBUST port connector location is provided for user expansion. This port provides the ROBUST Nexus 51 pin location that applies the GLENAIR MR7580-51P2BNU connector.

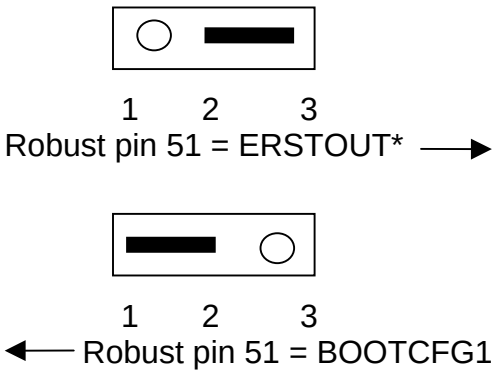
ROBUST Port

Pin #	Signal	Pin #	Signal	Pin #	Signal
1	+V	19	MDO0	36	GND
2	+V	20	GND	37	MDO4
3	B_VSTBY1	21	MCKO	38	GND
4	NXS35 TP	22	GND	39	MDO5
5	TDO	23	EVTO*	40	GND
6	B_RDY*	24	GND	41	MDO6
7	B_RESET*	25	MSEO0*	42	GND
8	B_+3.3V	26	MDO9	43	MDO7
9	B_EVTI*	27	MDO1	44	GND
10	GND	28	GND	45	MDO8
11	B_JCOMP	29	MDO2	46	GND
12	GND	30	GND	47	MDO10
13	B_TMS	31	MDO3	48	GND
14	GND	32	GND	49	MDO11
15	B_TDI	33	NXS29 TP	50	GND
16	GND	34	GND	51	JP1 pin 2
17	B_TCK	35	MSEO1*		
18	GND				

Notes:
1) NXS29 and NXS35 signals are also connected to the NEXUS connector.
2) Signals followed by a “*” symbol are active logic low.

JP1 Option

JP1 provides signal selection for the Robust Nexus connector pin 51. Position 1-2 provides the BOOTCFG1 signal and position 2-3 provides the ERSTOUT* signal.



MPC5553 I/O HEADER RING

MPC5553 I/O signals are provided by the I/O header ring. The header ring consists of .1 inch grid pins organized in 4 rows for each side of the MPC5553 device. Each row reflects the corresponding location of the MPC5553 device BGA package ball ring. Signals indicated are the DEMO board primary function.

A1 – AF4 HEADER

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
A1	GND	A2	VSTBY	A3	AN37	A4	AN11
B1	VDD	B2	GND	B3	AN36	B4	AN39
C1	3.3V	C2	VDD	C3	GND	C4	AN8
D1	TPU_A30	D2	TPU_A31	D3	VDD	D4	GND
E1	TPU_A28	E2	TPU_A29	E3	5V	E4	VDD
F1	TPU_A24	F2	TPU_A27	F3	TPU_A26	F4	5V
G1	TPU_A23	G2	TPU_A22	G3	TPU_A25	G4	TPU_A21
H1	TPU_A20	H2	TPU_A19	H3	TPU_A18	H4	TPU_A17
J1	TPU_A16	J2	TPU_A15	J3	TPU_A14	J4	TPU_A13
K1	TPU_A12	K2	TPU_A11	K3	TPU_A10	K4	TPU_A9
L1	TPU_A8	L2	TPU_A7	L3	TPU_A6	L4	TPU_A5
M1	TPU_A4	M2	TPU_A3	M3	TPU_A2	M4	TPU_A1
N1	BDIP*	N2	TEA*	N3	TPU_A0	N4	TCRCLK_A
P1	CS3*	P2	CS2*	P3	CS1*	P4	CS0*
R1	WE3*	R2	WE2*	R3	WE1*	R4	WE0*
T1	3.3V	T2	TSIZ0	T3	RD_WR	T4	3.3V
U1	A16	U2	TSIZ1	U3	TA*	U4	3.3V
V1	A18	V2	A17	V3	TS*	V4	A8
W1	A20	W2	A19	W3	A9	W4	A10
Y1	A22	Y2	A21	Y3	A11	Y4	3.3V
AA1	A24	AA2	A23	AA3	A13	AA4	A12
AB1	3.3V	AB2	A25	AB3	A15	AB4	A14
AC1	A26	AC2	A27	AC3	A31	AC4	GND
AD1	A28	AD2	A30	AD3	GND	AD4	VDD
AE1	A29	AE2	GND	AE3	VDD	AE4	CRS
AF1	GND	AF2	VDD	AF3	TX_CLK	AF4	TX_ER

A22 – D5 HEADER

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
A22	MDO11	B22	MDO7	C22	MDO3	D22	5V
A21	GPIO205	B21	MDO10	C21	MDO6	D21	MDO2
A20	x	B20	x	C20	MDO9	D20	MDO5
A19	x	B19	x	C19	x	D19	x
A18	x	B18	x	C18	x	D18	x
A17	x	B17	x	C17	x	D17	x
A16	ETRIG1	B16	ETRIG0	C16	x	D16	x
A15	AN15	B15	AN14	C15	AN13	D15	AN12
A14	VSSA	B14	VSSA	C14	VDDA0	D14	5V
A13	AN35	B13	AN32	C13	AN33	D13	AN34
A12	AN28	B12	AN31	C12	AN30	D12	AN29
A11	AN27	B11	AN26	C11	AN25	D11	AN24
A10	AN23	B10	AN22	C10	VRL	D10	AN6_DAN3+
A9	VRH	B9	x	C9	AN7_DAN3-	D9	AN2_DAN1+
A8	AN5_AND2-	B8	AN4_AND2+	C8	AN3_DAN1-	D8	AN18
A7	AN1_AND0-	B7	AN0_AND0+	C7	AN21	D7	AN10
A6	AN16	B6	AN20	C6	VSSA	D6	AN9
A5	VDDA1	B5	AN19	C5	AN17	D5	AN38

A23– AF26 HEADER

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
A23	MDO8	A24	VDD	A25	3.3V	A26	GND
B23	MDO4	B24	MDO0	B25	GND	B26	3.3V
C23	MDO1	C24	GND	C25	3.3V	C26	VDD
D23	GND	D24	3.3V	D25	TCK	D26	TDI
E23	3.3V	E24	TMS	E25	TDO	E26	TEST*
F23	MSEO0*	F24	JCOMP	F25	EVTI*	F26	EVTO*
G23	MSEO1*	G24	MCKO	G25	GPIO204	G26	x
H23	RDY*	H24	GPIO203	H25	x	H26	x
J23	5V	J24	x	J25	x	J26	x
K23	x	K24	x	K25	x	K26	x
L23	x	L24	x	L25	x	L26	x
M23	x	M24	x	M25	x	M26	SIN_B
N23	SOUT_B	N24	PCS_B3	N25	PCS_B0	N26	PCS_B1
P23	SIN_D	P24	PCS_B4	P25	SCK_B	P26	PCS_B2
R23	PCS_B5	R24	PCS_C5	R25	PCS_C2	R26	PCS_C1
T23	PCS_B2	T24	PCS_D2	T25	SCK_D	T26	5V
U23	SOUT_D	U24	TXDA	U25	PCS_B3	U26	3.3V
V23	CNTX_C	V24	RXDA	V25	RSTOUT*	V26	RSTCFG*
W23	RXDB	W24	CNRX_C	W25	TXDB	W26	RESET*
Y23	WKPCFG	Y24	BOOTCFG1	Y25	GND	Y26	GND
AA23	5V	AA24	PLLCFG1	AA25	BOOTCFG0	AA26	x (EXTAL)
AB23	VDD	AB24	x (VRCCTL)	AB25	PLLCFG0	AB26	x (XTAL)
AC23	GND	AC24	VDD	AC25	VRC33	AC26	x (VDDSYN)
AD23	NC2	AD24	GND	AD25	VDD	AD26	3.3V
AE23	3.3V	AE24	CLKOUT	AE25	GND	AE26	VDD
AF23	PCS_C4	AF24	3.3V	AF25	ENGCLK	AF26	GND

AC22– AF5 HEADER

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
AC22	NC11	AD22	3.3V	AE22	CNRX_A	AF22	PCS_C3
AC21	3.3V	AD21	CNTX_A	AE21	EMIOS23	AF21	EMIOS20
AC20	5V	AD20	EMIOS22	AE20	EMIOS19	AF20	EMIOS18
AC19	EMIOS21	AD19	EMIOS17	AE19	EMIOS16	AF19	EMIOS14
AC18	EMIOS12	AD18	EMIOS15	AE18	EMIOS13	AF18	EMIOS11
AC17	EMIOS8	AD17	EMIOS10	AE17	EMIOS9	AF17	EMIOS7
AC16	EMIOS2	AD16	EMIOS6	AE16	EMIOS5	AF16	EMIOS4
AC15	D14	AD15	EMIOS3	AE15	EMIOS1	AF15	EMOS0
AC14	D12	AD14	D15	AE14	MDIO	AF14	BB*
AC13	3.3V	AD13	D13	AE13	MDC	AF13	D7
AC12	D10	AD12	D11	AE12	OE*	AF12	D5
AC11	D8	AD11	D9	AE11	D6	AF11	3.3V
AC10	RXD3	AD10	GPIO207	AE10	D4	AF10	D3
AC9	RXD2	AD9	3.3V	AE9	D2	AF9	D1
AC8	3.3V	AD8	RXD1	AE8	D0	AF8	GPIO206
AC7	TXD1	AD7	TXD2	AE7	TXD3	AF7	RXD0
AC6	TX_EN	AD6	RX_DV	AE6	RX_ER	AF6	TXD0
AC5	VDD	AD5	COL	AE5	RX_CLK	AF5	3.3V

Note: Indicated as AF22 / AF5 on DEMO board.